UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,732	09/30/2003	David Arnold Luick	ROC920030254US1	6370

7590 12/27/2005

Robert R. Williams
IBM Corporation, Dept. 917
3605 Highway 52 North
Rochester, MN 55901-7829

EXAMINER	
GU, SHAWN X	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 12/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/675,732	LUICK, DAVID ARNOLD	
	Examiner	Art Unit	
	Shawn Gu	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-23* is/are allowed.

6)☒ Claim(s) *24,25 and 29-32* is/are rejected.

7)☒ Claim(s) *26-28,33 and 34* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

The disclosure is objected to because of the following informalities:

The specification contains numerous omissions of serial numbers referenced by the Applicant, such as those on Pages 1 and 6 of the specification.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 24 and 32 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As for claims 24 and 32, it is unclear to the Examiner if the "a plurality of said page table entries" refers to the previously stated "plurality of page table entries", or some other group of page table entries. It would be more appropriate to modify the phrase as "the plurality of said page table entries", and the Examiner is rejecting the claims as such.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 24, 25, 29, 30 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Doing et al. [6,161,166] (hereinafter "Doing"), in further view of Kedem et al. [6,134,643] (hereinafter "Kedem") and Schumann et al. [6,012,106] (hereinafter "Schumann").

As for claim 24, Doing teaches a digital data processing device, comprising:

at least one processor (Fig 1A and Fig 2, 101 CPU);

a memory (Fig 1A and Fig 1B, 102 Main Memory), said memory containing a page table, said page table having a plurality of page table entries corresponding to addressable pages (Fig 8, 822 Page Table); and

at least one cache for temporarily storing data from said memory (Fig 1A, 108 L2 cache). Doing does not teach a pre-fetch engine or persistent reference history data contained in each page table entry.

However, Kedem teaches a digital data processing device which comprises a pre-fetch engine (Fig 1, combination of 30 Prefetch Controller, 40 Prediction Table, and 35 Prefetch Buffer), said pre-fetch engine pre-fetching data from addressable pages to

at least one cache using persistent reference history data with respect to the corresponding addressable page, said persistent reference history data being maintained throughout the life of the corresponding addressable page in memory (Col 3, Lines 22-42), in order to improve access latency without significantly affecting the operation of the processor (Col 3, Lines 10-21). Therefore, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention that Doing digital data processing device could incorporate Kedem's pre-fetch engine and persistent reference history data to improve access latency. Yet, Kedem does not teach that the persistent history data used by the pre-fetch engine is contained in each of a plurality of said page table entries.

However, Schumann teaches a digital data processing device which comprises pre-fetching data from addressable pages using persistent reference history data with respect to the corresponding addressable page, the persistent reference history data contained in a plurality of page table entries in a page table, the persistent reference history data being maintained throughout the life of the corresponding addressable page in memory (Fig 2, Prefetch Length in 21 Page Table; Col 4, Lines 18-63), with the intention to reduce the number of wait states and improve access time (see Abstract), and further improve cache throughput (Col 1, Lines 60-65). Furthermore, keeping the persistent reference history data in cache as disclosed in Kedem increases design complexity since that further require deciding the size of the prediction table and replacement algorithm (Kedem, Col 3, Lines 43-49). Therefore, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention that

Doing device in combination with that of Kedem's, would reduce number of wait states, improve access time and cache throughput, and further reduce design complexity, if further includes Schumann's design.

As for claims 25 and 32, Doing further teaches the said digital data processing system comprises a plurality of processors (Fig 1B, 101A-101D CPUs; Col 6, Lines 15-19), and it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention that the said persistent history data is based on reference events occurring in said plurality of processors, since the plurality of processors all make references to the same memory (Fig 1B, 102 Main Memory).

As for claim 29, Doing further teaches the said digital data processing device comprises a plurality of caches at a plurality of cache levels (Fig 1A, 106 L1 I-cache, 107 L1 D-cache, and 108 L2 cache), and it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention that said pre-fetch engine taught in claim 24 pre-fetches data to different cache levels, as both L1 and L2 caches access the same memory (Fig 1B, 102 Main Memory) which contains the page table that holds persistent reference history data for pre-fetching to cache.

As for claim 30, Doing further teaches the digital data processing system further comprises:

an address translation mechanism which translates effective addresses in an address space of a task executing on said at least one processor to virtual addresses in a global address space of said digital processing system, and translates said virtual addresses to real addresses corresponding to physical memory locations in said memory (Figs 4-8).

Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Doing in combination with Kedem and Schumann, in further view of "Computer Architecture A Quantitative Approach" [by David A. Patterson and John L. Hennessy] (hereinafter "Patterson") and Chauvel [US 6,957,315 B2] (hereinafter "Chauvel").

As for claim 31, Doing in combination of Kedem and Schumann already substantially disclosed the claim as described above, but do not particularly point out that the said pre-fetch engine pre-fetches address translation data into at least one address translation cache structure of said address translation mechanism. However, Patterson discloses that in a virtual memory system such as that of Doing's, a TLB (Translation Look-aside Buffer) that contains address translation data is included to improve address translation latency (Pages 445-446). Chauvel further teaches pre-fetching TLB entries to prevent TLB misses (Col 8, Lines 18-22).

Therefore it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention that Patterson and Chauvel's teachings can be

combined with those of Doing, Kedem, and Schumann, in order to improve address translation latency and prevent TLB misses.

Allowable Subject Matter

Claims 26-28, 33, and 34 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for allowance:

Claims 1 and 17 are allowed as the combination of above cited references Doing, Kedem, and Schumann teaches every limitation of the claims except that the reference history data in the combined references are not contained in the page table entries, respectively for each of a plurality of cacheable sub-units of the corresponding addressable pages. Instead the reference history data in the combined references is for the entire page as a whole.

Claim 11 is allowed as the combined references Doing, Kedem, and Schumann teach every limitation of the claim except that the counter is only an up-counter instead

of an un-down counter (Kedem, Fig 2, Item 55), and there is no second type of event to trigger the decrement of the counter.

Claims 2-10, 12-16, and 18-23 are allowed as they are depended on claims 1, 11, and 17.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shawn Gu whose telephone number is (571) 272-0703. The examiner can normally be reached on 9am-5pm, Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571)272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shawn X Gu
Assistant Examiner
Art Unit 2189

21 December 2005

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER